MMBT5401LT1G

High Voltage Transistor

PNP Silicon

ON Semiconductor®

http://onsemi.com

Features

- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

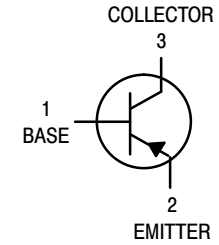
Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	−150	Vdc
Collector − Base Voltage	V_{CBO}	−160	Vdc
Emitter − Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current − Continuous	I_C	−100	mAdc
Electrostatic Discharge	ESD	HM < 1000 MM > 400	V V

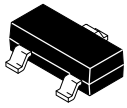
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board (Note 1) T_A = 25°C Derate Above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate (Note 2) T_A = 25°C Derate Above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

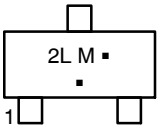
1. FR−5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in 99.5% alumina.





SOT−23 (TO−236)
CASE 318
STYLE 6

MARKING DIAGRAM



2L = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MMBT5401LT1G	SOT−23 (Pb−Free)	3000 Tape & Reel
MMBT5401LT3G	SOT−23 (Pb−Free)	10,000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector – Emitter Breakdown Voltage (I_C = −1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	−150	–	Vdc
Collector – Base Breakdown Voltage (I_C = −100 μAdc, I_E = 0)	$V_{(BR)CBO}$	−160	–	Vdc
Emitter – Base Breakdown Voltage (I_E = −10 μAdc, I_C = 0)	$V_{(BR)EBO}$	−5.0	–	Vdc
Collector Cutoff Current (V_{CB} = −120 Vdc, I_E = 0) (V_{CB} = −120 Vdc, I_E = 0, T_A = 100°C)	I_{CES}	– –	−50 −50	nAdc μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = −1.0 mAdc, V_{CE} = −5.0 Vdc) (I_C = −10 mAdc, V_{CE} = −5.0 Vdc) (I_C = −50 mAdc, V_{CE} = −5.0 Vdc)	h_{FE}	50 60 50	– 240 –	–
Collector – Emitter Saturation Voltage (I_C = −10 mAdc, I_B = −1.0 mAdc) (I_C = −50 mAdc, I_B = −5.0 mAdc)	$V_{CE(sat)}$	– –	−0.2 −0.5	Vdc
Base – Emitter Saturation Voltage (I_C = −10 mAdc, I_B = −1.0 mAdc) (I_C = −50 mAdc, I_B = −5.0 mAdc)	$V_{BE(sat)}$	– –	−1.0 −1.0	Vdc
SMALL−SIGNAL CHARACTERISTICS				
Current – Gain — Bandwidth Product (I_C = −10 mAdc, V_{CE} = −10 Vdc, f = 100 MHz)	f_T	100	300	MHz
Output Capacitance (V_{CB} = −10 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	–	6.0	pF
Small Signal Current Gain (I_C = −1.0 mAdc, V_{CE} = −10 Vdc, f = 1.0 kHz)	h_{fe}	40	200	–
Noise Figure (I_C = −200 μAdc, V_{CE} = −5.0 Vdc, R_S = 10 Ω, f = 1.0 kHz)	NF	–	8.0	dB

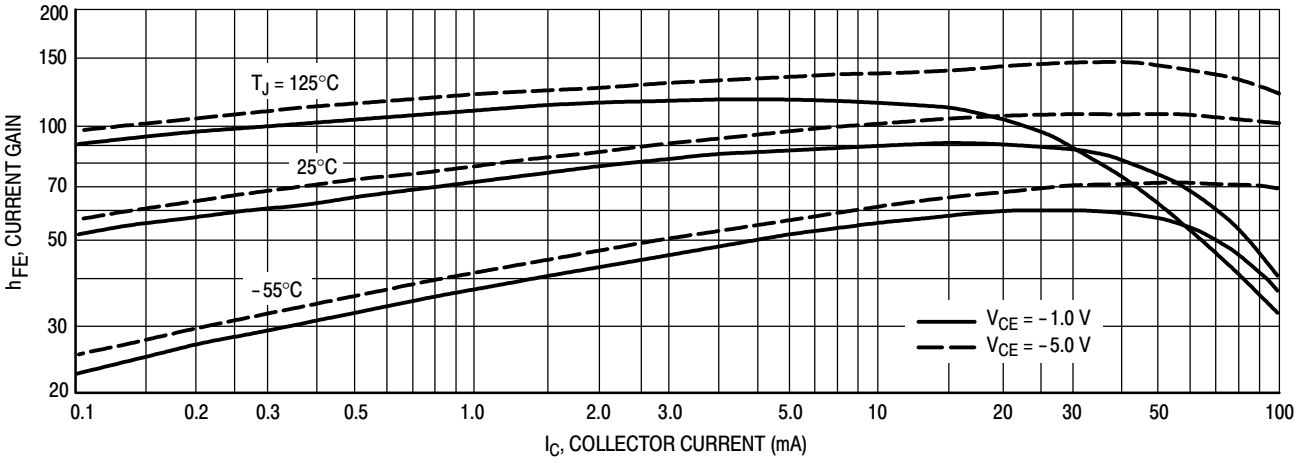


Figure 1. DC Current Gain

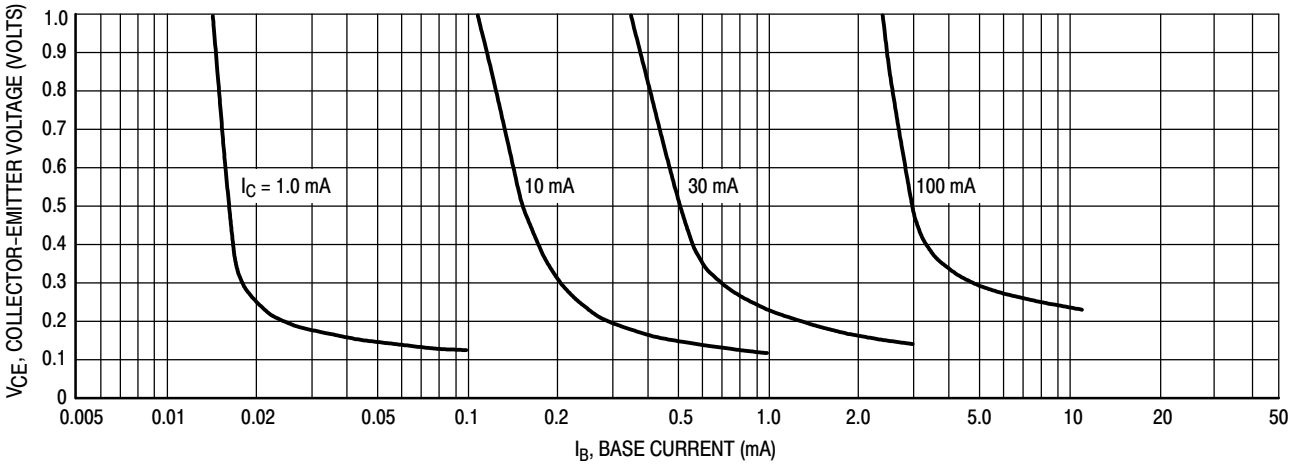


Figure 2. Collector Saturation Region

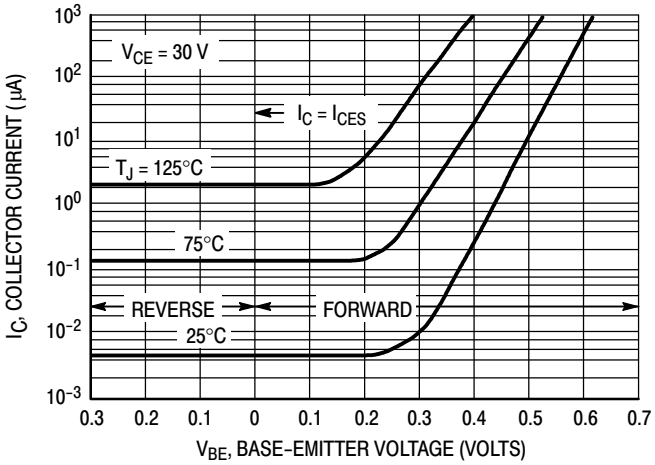


Figure 3. Collector Cut−Off Region

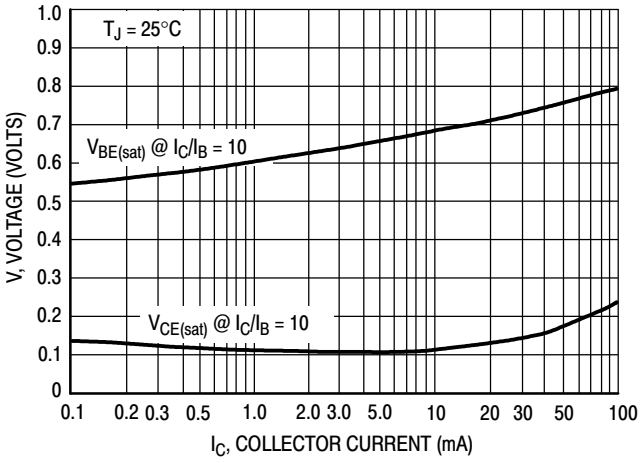


Figure 4. “On” Voltages

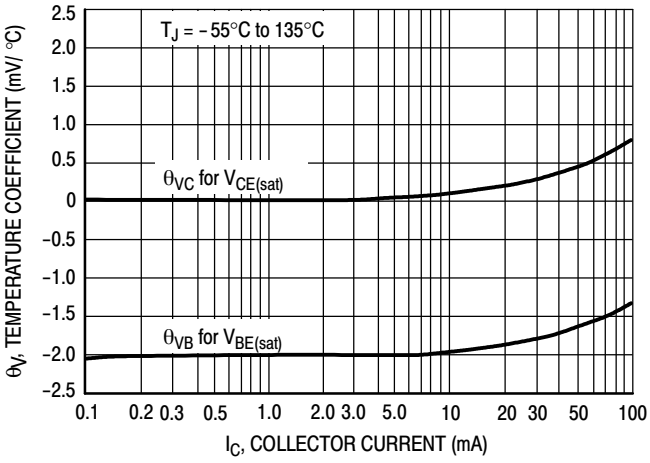


Figure 5. Temperature Coefficients

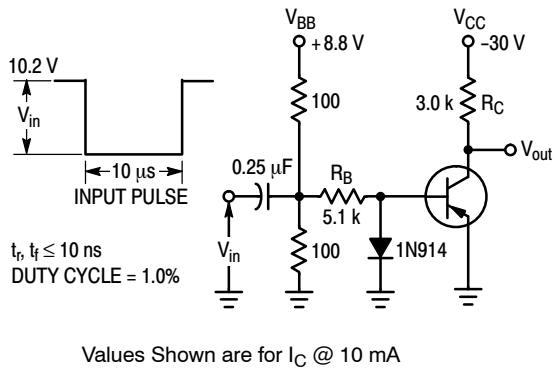


Figure 6. Switching Time Test Circuit

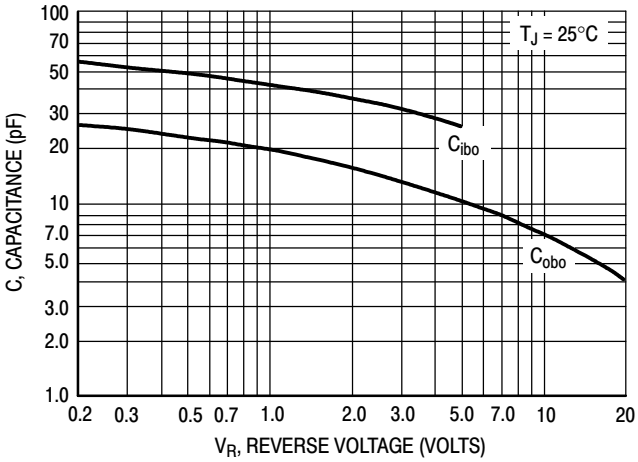


Figure 7. Capacitances

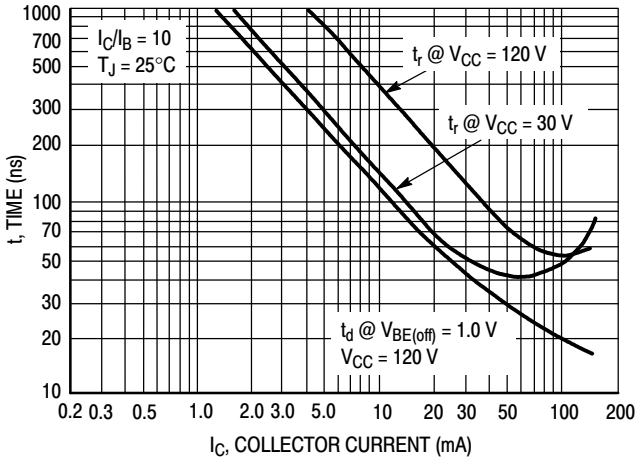


Figure 8. Turn−On Time

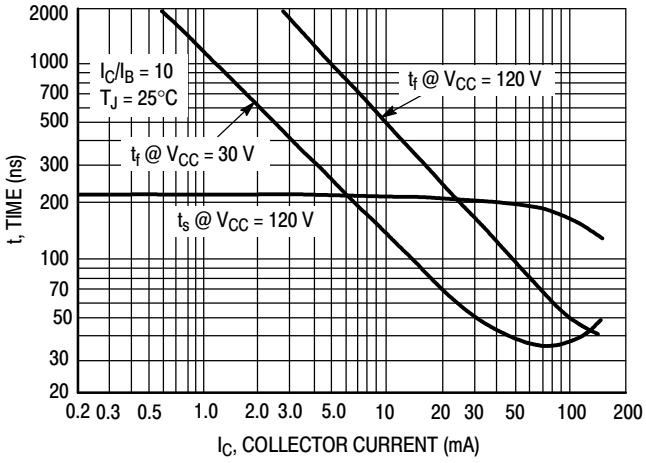
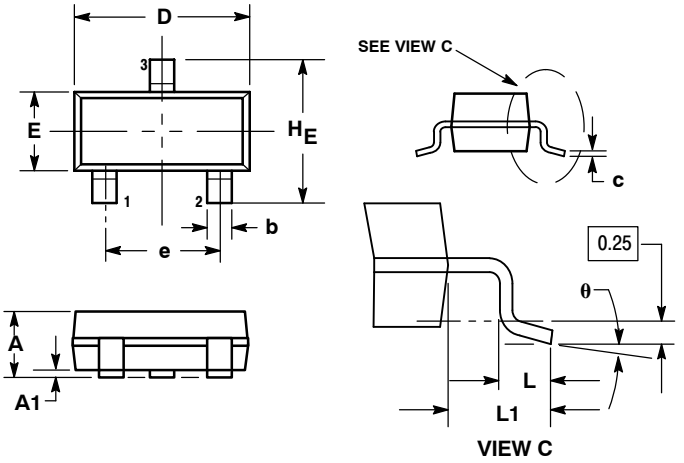


Figure 9. Turn−Off Time

PACKAGE DIMENSIONS

SOT−23−3 (TO−236)
CASE 318−08
ISSUE AN

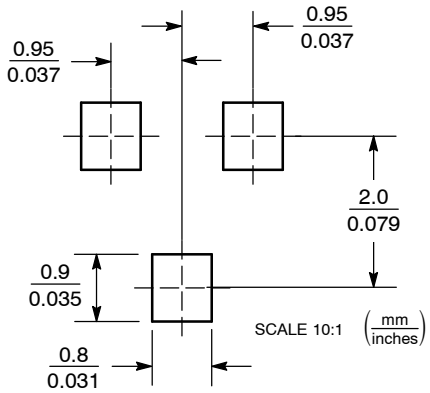


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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